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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
CHEN, ALAN S	

ART UNIT	PAPER NUMBER
2182	5

DATE MAILED: 04/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/659,914	VRANCIC ET AL.	
	Examiner	Art Unit	
	Alan S Chen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2,4-15 and 32* is/are allowed.

6)☒ Claim(s) *16-21,24,30 and 31* is/are rejected.

7)☒ Claim(s) *22,23 and 25-29* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED FINAL ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 16-21, 24, 30 and 31 are rejected under 35 USC 103(a) as being unpatentable over No. 5,659,749 to Mitchell et al. (hereafter Mitchell) in view of No. 6,006,286 to Baker et al. (hereafter Baker).

3. As per claim 16, Mitchell discloses a system for transferring data over a communication medium (Fig. 3), the system comprising: a data acquisition device (Fig. 3, element 104) coupled to a first end of the communication medium (Fig. 3, element 106); and a host computer system (Fig. 3, element 102) coupled to a second end of the communication medium (Fig. 3, 106), wherein the host computer is operable to communicate through the communication medium to the data acquisition device; wherein the host computer system is operable to prepare a plurality of transfer commands (Fig. 3, element 108) and transfer the commands to the link buffer (Column 5, lines 28-50) in a double buffered fashion (link buffer can hold more than one command), wherein each of the plurality of transfer commands specifies a transfer of data between the data acquisition device and the host computer system.

Mitchell does not disclose expressly the host computer preparing a plurality of transfer links wherein each of the plurality of transfer links specifies a transfer of data between the DAQ device and the host computer.

Baker discloses a system for transferring data over a communication medium (Fig. 1) the system comprising the host computer preparing a plurality of transfer links (Fig. 20), wherein each of the plurality of transfer links specifies a transfer of data between the data acquisition device and the host computer (Fig. 20, elements 456, 470 and 486).

Mitchell and Baker are analogous art because they are from the same field of endeavor in transferring data over a detachable link/cable.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Mitchell with Baker to use the transfer link data structure.

The suggestion/motivation for doing so would have been to provide the advantage of using a minimal number of input and output accesses to the data transfer device memory (Column 3) thereby increasing efficiency and performance of the system.

Therefore, it would have been obvious to combine Baker with Mitchell for the benefit of minimizing the number of input and output accesses to the data transfer device memory.

4. As per claim 17, Mitchell further disclose the bi-directional nature of the transfers between the host and DAQ device, where transferring data from the host to the DAQ device requires a request/fetch from the DAQ device.

5. As per claim 18, Mitchell further discloses the buffer queue having the ability to store a plurality of transfer commands (Column 5, lines 28-50), thereby providing a double or more buffering mechanism.

6. As per claims 30 and 31, Mitchell combined with Baker disclose claim 16. Baker further discloses use of IEEE 1394 bus (Fig. 1) and using the PCI protocol for part of the hardware

interface. Furthermore, to bridge the PCI and 1394 protocol, the system uses a PCI/1394 translator (Fig. 1, element 18 and 20).

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Mitchell with Baker to use 1394 and PCI protocols.

The suggestion/motivation for doing so would have been the PCI local bus is the de facto standard in current personal computers while IEEE 1394 is very popular currently since it provides high transfer speeds and is advanced relative to the other serial data links that currently exist (Column 1, lines 30-45).

Therefore, it would have been obvious to combine Baker with Mitchell for the benefit of going with established and quality communication buses.

7. As per claim 19, Mitchell further discloses the system of claim 18, wherein the host computer system is further operable to: configure the DAQ for I/O (Fig. 3, element 108) and initiate a data I/O operation on the DAQ device, after the host computer transfers to it data.

8. As per claims 20 and 21, Mitchell further discloses the methods of claims 19, wherein the host computer being operable to initiate the data I/O operation (Fig. 3, element 108) comprising the host computer being operable to a DAQ process on the DAQ device; wherein the data acquisition device comprises a DMA controller (Fig. 5, element 221); and wherein the DAQ device being capable of executing a plurality of commands (Column 5, lines 28-50) being able to transmit and receive data. The DAQ device (Fig. 5) receives the data from the expansion card (Fig. 4) and processing/notification is done by the DMA transfer logic (Fig. 5, element 221).

9. As per claim 24, Mitchell combined with Baker disclose the system of claim 16, wherein each link comprises one source address (Fig. 20, element 474), a count of the number of bytes in

the transfer (Fig. 20, element 466, address 0x24), and a pointer to a subsequent link (Fig. 20, element 466, address 0x0).

Response to Arguments

10. Any rejection not addressed in this Office Action has been withdrawn.

11. Applicant's arguments filed 03/15/2004, with respect to the rejection(s) of claim(s) 16-21, 24, 30 and 31 under U.S.C. §103(a) have been fully considered but they are not persuasive. Examiners reasons are given below.

Rejections under 35 U.S.C. 103(a)

Claims 16-21, 24, 30 and 31

12. Applicant argues that neither Mitchell nor Baker provides a motivation to combine and further that if combined, it would not produce the Applicant's invention. It is clear that Mitchell and Baker both deal with transfer of data/commands from one location to another, specifically dealing with DMA transfers, where there is a delay between the actual execution of the transferred data/commands due to discrepancies between the transfer rate of the host and the receive rate of the peripheral device and therefore requiring a queue and a data structure. Baker shows a data structure (Fig. 20) that enables efficient transfer of data between the host and device. It is obvious from the need to optimize DMA transfers and queue data structuring to combine Baker and Mitchell.

13. As per claim 16-21,24,30 and 31, applicant argues of page 16, last paragraph of his amendment "...host computer is operable to prepare a plurality of transfer links and transfer a plurality of transfer links to the link buffer of the data acquisition device in a double buffered fashion...". The term "double buffered fashion" as claimed is simply to broadly disclosed by the

applicant. Examiner wishes to point out that one definition given by the applicant of double buffering was stated in applicants cancelled claim 3, where the peripheral DAQ device executes a first plurality of transfer links from a first portion of the buffer while the host computer transfers a second plurality of transfer links to a second portion of the link buffer. This definition of double buffering is precisely what Mitchell discloses in Column 5, lines 25-35. The DMA transfer logic on the peripheral side (Fig. 5, element 221) has a transfer queue that stores transfer commands as they are received and are executed as they arrive at the head of the queue. Here, the head of the queue (technically the first element of the queue stack) is the first portion of the buffer, while the rest of the queue is not executed immediately and are stored in order, as the commands from the arrive from the host, is the second portion of the queue. The double buffering fashion described by the applicant reads upon a First-In-First-Out type queue, which is well known in the art.

Allowable Subject Matter

14. Claims 22,23 and 25-29 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

15. Claims 1,2,4-15 and 32 are allowed.

As per claims 1,2 and 4-15 the following is the statement of reasons for the indication of allowable subject matter: The prior art disclosed by the applicant and cited by the Examiner fail to teach or suggest, alone or in combination, a data acquisition device that executes part of the transfer link that is sent to the DAQ device while the other part is still on the host side, and once

another part of the transfer link is transferred, thereupon executing an already transferred transfer link, such that the execution and transfer are done concurrently.

As per claim 32, the following is the statement of reasons for the indication of allowable subject matter: The prior art disclosed by the applicant and cited by the Examiner fail to teach or suggest, alone or in combination, for each transfer node of the linked list of transfers, the true address of the transfer node corresponds to a virtual address of a buffer, wherein the buffer spans contiguous virtual addresses mapping to the physical memory of the host computer system, wherein an Nth transfer node corresponds to an Nth virtual address of the buffer.

Conclusion

16. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

17. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alan S Chen whose telephone number is 703-605-0708. The examiner can normally be reached on M-F 8:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A Gaffin can be reached on 703-308-3301. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

ASC
4/26/2004

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